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09/752,615	12/27/2000	Sung-min Yim	AB-1053 US	1304

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Attn: Mr. John Castellano  
Harness, Dickey & Pierce  
12355 Sunrise Valley Drive  
Suite 350  
Reston, VA 20191

EXAMINER

CLEARY, THOMAS J

ART UNIT PAPER NUMBER

2181

DATE MAILED: 07/21/2003

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Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Applicati n N .

09/752,615

Applicant(s)

YIM ET AL.

Examiner

Thomas J. Cleary

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 12/27/00.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-15 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 27 December 2000 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☒ Certified copies of the priority documents have been received in Application No. 09/752,615.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_ 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Drawings***

1. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.
2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: Number 53 in Figure 3. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.
3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the multiplexer of Claims 5 and 14 that transmits one of the column cycle signal and the read control signal to the gate of the second transistor must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

***Specification***

4. The disclosure is objected to because of the following informalities: On page 5, Line 25, the word "resistors" should be replaced with the word "registers".

Appropriate correction is required.

***Claim Rejections - 35 USC § 112***

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 3 and 13 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claims 3 and 13 use cyclic terminology in claiming that the controller activates the second transistor when the second transistor responds to the read control signal. Claim 13 further states that each controller separately activates the associated second transistor when cell data of the selected DQ block is transmitted to the data input/output lines via the first and second transistors, implying that the second transistor is deactivated and is only activated after it is used.

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7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 3 and 13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 3 and 13 use indefinite language in claiming that the controller activates the second transistor when the second transistor responds to the read control signal. Claim 13 further states that each controller separately activates the associated second transistor when cell data of the selected DQ block is transmitted to the data input/output lines via the first and second transistors, implying that the second transistor is deactivated and is only activated after it is used.

9. Claims 4, 5, and 6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

10. Claims 4, 5, and 6 recite the limitation "control" in Line 1 of Claim 4. There is insufficient antecedent basis for this limitation in the claim. The Examiner recommends changing the word "control" to "controller" and will assume said change for the purposes of evaluating prior art.

***Claim Rejections - 35 USC § 102***

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

12. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Tobin et al. Tobin et al. teach an output driver consisting of two transistors in series. The first transistor is connected to a reference voltage and is controlled by an input signal, which is analogous to the memory input of Claim 1. The second transistor is connected between the first transistor and the bus line, and is controlled by a control module signal, which is analogous to the column cycle signal of Claim 1 (See Column 10, Line 25 – Column 11, Line 14 and Figures 5 and 6 of Tobin et al.).

### ***Claim Rejections - 35 USC § 103***

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

14. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tobin et al. in view of Kametani. Tobin et al. suggest all the features of Claim 2 except deactivating the second transistor when a second set of blocks is selected for data output (See Column 10, Line 25 – Column 11, Line 14 and Figures 5 and 6 of Tobin et al.). Kametani teaches the use of a selective controller which can connect and disconnect one of a plurality of CPUs from a common bus (See Column 10, Lines 28-33 of Kametani). The CPUs of Kametani are analogous to the output driver of Claim 2. One of ordinary skill in the art at the time the invention was made would construct the output driver of Tobin et al. with the selective controller of Kametani, resulting in the invention of Claim 2, in order to minimize the capacitive load present on the bus line.

15. Claims 4 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tobin et al. in view of Garlepp et al. Tobin et al. suggest all the features of Claims 4 and 6 except the second transistor being responsive to a read control signal containing calibration information, and the calibration information being comprised of a current and a temperature characteristic (See Column 10, Line 25 – Column 11, Line 14 and Figures 5 and 6 of Tobin et al.). Garlepp et al. teach a type of memory device, known in the art, which can collect and store a variety of information pertaining to the characteristics of the memory bus, and which can be used to tune the performance of

the memory interface. (See Column 3, Lines 47 – 67 of Garlepp et al.). One of ordinary skill in the art at the time the invention was made would construct the output driver of Tobin et al. with the interface taught by Garlepp et al. resulting in the invention of Claim 4, in order to tune the performance of the memory interface, as suggested by Garlepp et al. (See Column 3, Lines 65 – 67 of Garlepp et al.).

16. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tobin et al. and Garlepp et al. in further view of Gervais et al. Tobin et al. and Garlepp et al. teach all the limitations of Claim 5 except the control unit comprised of a multiplexer which responds to a clock enable signal (See Column 10, Line 25 – Column 11, Line 14 and Figures 5 and 6 of Tobin et al. and See Column 3, Lines 47 – 67 of Garlepp et al.). Gervais et al. teach the use of a multiplexer which chooses between two input signals in response to a clock signal (See Column 4, Lines 62 – 67 of Gervais et al.). One of ordinary skill in the art at the time the invention was made would construct the memory module of Tobin et al. and Garlepp et al. with the clock-controlled multiplexer controller of Gervais et al. resulting in the invention of Claim 5, in order to provide a means for selecting the signal to be output by the controller.

17. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gillingham et al. in view of Tobin et al. and Kametani. Gillingham et al. teach the use of a memory subsystem comprising at least two semiconductor devices, a main bus for carrying the data and command information, and an output driver comprised of a single

transistor (See Figure 2a, Column 4, Lines 19-22, and Column 6 Lines 19-27 of Gillingham et al.). Gillingham et al. do not teach the use of an output driver comprised of two transistors that can be selectively disconnected from the bus. Tobin et al. teach the use of an output driver comprised of two transistors in which the first transistor is connected to a reference voltage and is responsive to an input signal and the second transistor is connected between the first transistor and the bus and is responsive to a control signal (See Column 10, Line 25 – Column 11, Line 14 and Figures 5 and 6 of Tobin et al.). Kametani teaches the use of a controller that can selectively connect and disconnect CPUs from a bus line (See Column 10, Lines 28-33 of Kametani). The CPUs of Kametani are analogous to the output drivers of Claim 7. One of ordinary skill in the art at the time the invention was made would construct the memory system of Gillingham et al. with the output driver of Tobin et al. and the selective controller of Kametani, resulting in the invention of Claim 7, in order to minimize the capacitance of the bus line, which in turn will minimize the power consumed by the device as well as minimize the degradation of the data being transmitted across the bus.

18. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gillingham et al., Tobin et al., and Kametani, in further view of Kohno. Gillingham et al., Tobin et al., and Kametani teach all the limitations of Claim 8 except the second transistors of all the output drivers being simultaneously activated (See Column 10, Line 25 – Column 11, Line 14 and Figures 5 and 6 of Tobin et al.; Figure 2a, Column 4, Lines 19-22, and Column 6 Lines 19-27 of Gillingham et al.; and Column 10, Lines 28-33 of

Kametani). Kohno teaches a semiconductor memory device in which all of the memory modules are simultaneously activated during a read operation (See Column 11, Lines 66 – 67 and Column 12, Lines 1 – 3 of Kohno). One of ordinary skill in the art at the time the invention was made would combine the memory module of Gillingham et al., Tobin et al., and Kametani with the memory module of Kohno, resulting in the invention of Claim 8, in order to produce a device which will send all read-out data to an external element simultaneously, as discussed in Kohno (See Column 11, Lines 61 – 65 of Kohno).

19. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gillingham et al., Tobin et al., and Kametani in further view of Gervais et al. Gillingham et al., Tobin et al., and Kametani teach all the limitations of Claim 9 except the multiplexer which responds to a clock enable signal (See Column 10, Line 25 – Column 11, Line 14 and Figures 5 and 6 of Tobin et al.; Figure 2a, Column 4, Lines 19-22, and Column 6 Lines 19-27 of Gillingham et al.; and Column 10, Lines 28-33 of Kametani). Gervais et al. teach the use of a multiplexer which chooses between two input signals in response to a clock signal (See Column 4, Lines 62 – 67 of Gervais et al.). One of ordinary skill in the art at the time the invention was made would construct the memory module of Tobin et al. and Garlepp et al. with the clock-controlled multiplexer of Gervais et al. resulting in the invention of Claim 5, in order to provide a means for selecting the signal to be output to the second transistor.

20. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gillingham et al., Tobin et al., and Kametani in further view of Garlepp et al. Gillingham et al., Tobin et al., and Kametani teach all the limitations of Claim 10 except for the characteristics of the data input/output line being an output current characteristic and a temperature characteristic (See Column 10, Line 25 – Column 11, Line 14 and Figures 5 and 6 of Tobin et al.; Figure 2a, Column 4, Lines 19-22, and Column 6 Lines 19-27 of Gillingham et al.; and Column 10, Lines 28-33 of Kametani). Garlepp et al. teach a type of memory device, known in the art, which can collect and store a variety of information pertaining to the characteristics of the memory bus, and which can be used to tune the performance of the memory interface. (See Column 3, Lines 47 – 67 of Garlepp et al.). One of ordinary skill in the art at the time the invention was made would construct the output driver of Tobin et al. with the interface taught by Garlepp et al. resulting in the invention of Claim 10, in order to tune the performance of the memory interface, as suggested by Garlepp et al. (See Column 3, Lines 65 – 67 of Garlepp et al.).

21. Claims 11 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gillingham et al. in view of Tobin et al. and Garlepp et al. Gillingham et al. teach the use of a memory system comprising a plurality of memory devices and a plurality of output drivers comprised of a single transistor and a controller. Gillingham et al. do not teach the use of an output driver comprised of two transistors (See Figure 2a; Column 4, Lines 19-22; and Column 6 Lines 19-27 of Gillingham et al.). Tobin et al. teach the use of an output driver comprised of two transistors in which the first transistor is

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connected to a reference voltage and is responsive to an input signal and the second transistor is connected between the first transistor and the bus and is responsive to a control signal. Garlepp et al. teach a type of memory device, known in the art, which can collect and store a variety of information pertaining to the characteristics of the memory bus, and which can be used to tune the performance of the memory interface. (See Column 3, Lines 47 – 67 of Garlepp et al.). One of ordinary skill in the art at the time the invention was made would construct the memory system of Gillingham et al. with the output driver of Tobin et al. and the interface taught by Garlepp et al. resulting in the invention of Claim 11, in order to tune the performance of the memory interface, as suggested by Garlepp et al. (See Column 3, Lines 65 – 67 of Garlepp et al.) and to minimize the capacitance of the bus line, which in turn will minimize the power consumed by the device as well as minimize the degradation of the data being transmitted across the bus.

22. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gillingham et al., Tobin et al., and Garlepp et al. in further view of Kametani. Gillingham et al., Tobin et al., and Garlepp et al. teach all the restrictions of Claim 12 except for deactivation the second transistors of the output drivers in unselected blocks (See Column 10, Line 25 – Column 11, Line 14 and Figures 5 and 6 of Tobin et al.; Figure 2a, Column 4, Lines 19-22, and Column 6 Lines 19-27 of Gillingham et al.; and Column 3, Lines 65 – 67 of Garlepp et al.). Kametani teaches the use of a controller that can selectively connect and disconnect CPUs from a bus line (See Column 10, Lines 28-33

of Kametani). The CPUs of Kametani are analogous to the second transistors of the output drivers of Claim 12. One of ordinary skill in the art at the time the invention was made would combine the semiconductor memory device of Gillingham et al., Tobin et al., and Garlepp et al. with the controller of Kametani, resulting in the invention of Claim 12, in order to minimize the capacitive load on the bus line.

23. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gillingham et al. in view of Tobin et al. and Garlepp et al. in further view of Gervais et al. Gillingham et al. in view of Tobin et al. and Garlepp et al. teach all the limitations of Claim 5 except the control unit comprised of a multiplexer which responds to a clock enable signal (See Figure 2a; Column 4, Lines 19-22; and Column 6 Lines 19-27 of Gillingham et al.). Gervais et al. teach the use of a multiplexer which chooses between two input signals in response to a clock signal (See Column 4, Lines 62 – 67 of Gervais et al.). One of ordinary skill in the art at the time the invention was made would construct the memory module of Tobin et al. and Garlepp et al. with the clock-controlled multiplexer controller of Gervais et al. resulting in the invention of Claim 5, in order to provide a means for selecting the signal to be output by the controller.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Cleary whose telephone number is 703-305-5824. The examiner can normally be reached on Monday-Thursday (8-5:30), Alt. Fridays (8-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7249 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-5631.

tjc  
July 11, 2003



MARK H. RINEHART  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2100